PLEASE AMEND THE SPECIFICATION AS INDICATED BELOW:

Page 1, paragraph beginning at line 10:

This invention relates to a memory module and a memory system, particularly, to a memory system having a plurality of memory modules connected to a memory controller in a ~~stub~~ stab connection.

Page 6, paragraph beginning at line 22:

If the memory modules as shown in Fig. 1 are connected to the memory controller with a common transmission bus line in a ~~stub~~ stab connection, the memory system has a simple arrangement of wiring. In addition, it is possible to widen bus width of the common transmission bus line.

Page 6, paragraph beginning at line 27:

However, the stab connection has some or many branch points. Accordingly, it is easy to cause reflection of a transmission signal at each of the branch points on the common transmission bus line. The reflected signals become considerable when a transmission rate of the transmission signal becomes high. Thus, the ~~stub~~ stab connection limits an operation speed of the memory system using the memory modules as shown in Fig. 1.

Page 7, paragraph beginning at line 9:

In Fig. 3, four transmission lines each of which has wiring impedance Z0 are connected to one another at a branch point through respective ~~stub~~ stab resistors each of which has resistance Rs. When attention is focused on one of the transmission ~~liens~~ lines, the remaining three transmission lines are regarded as branches diverged from the focused transmission line. That is, the star connection of Fig. 3 comprises a transmission line with three (N=3) branches.

Page 7, paragraph beginning at line 26:

Thus, in the star connection of Fig. 3, a signal transmitted from any direction is not reflected at the branch point when the resistance Rs of the ~~stub~~ stab resistors satisfies the equation (3). That is, the transmission line having N of branches can be formed by adopting the resistance Rs found by using the equation (3).

Page 8, paragraph beginning at line 3:

Additionally, Japanese Unexamined Patent Publication No. 2001-84070 discloses a method for finding resistance of two ~~stub~~ stab resistors (N=2) in a transmission line having two branches. However, the method is not applicable to a case where the number of branches is equal to or more than three (N?3). Furthermore, the method is for a liquid crystal display panel and the publication does not suggest that it is applicable to a memory system, especially a high speed memory system. The method is on condition that termination resistors are not connected to ends of the wires and that reflection occurs at the ends of the wires. Furthermore, the method is impossible to be applied to the memory system because it fixes a characteristic impedance of one of the wires at first and then decide characteristics impedance of the remaining two wires and resistors.

Page 11, paragraph beginning at line 28:

In each of the memory systems 60 and 70, the module transmission bus lines 53 and the motherboard transmission bus line 63 or 73 is used for an IO bus line (or a bi-directional bus). Each of the memory chips 51 comprises a driver and a receiver connected to the IO bus line. Each of the memory controllers 61 and 71 similarly comprises a driver and a receiver connected to the IO ~~bas~~ bus line. In Fig. 6, two sets of the driver and the receiver are designated by small triangles in the memory controller 61 and one of the memory chips 52. Similarly, Fig. 7 shows other two sets of the driver and the receiver with small triangles.

Page 15, paragraph beginning at line 10:

In Fig. 13, the memory module 130 comprises a memory board 131, nine memory chips 132, module IO ~~bas~~ bus lines 133, terminating resistors 134, stab resistors 135, and pins 136.

Page 15, paragraph beginning at line 13:

The memory board 131 is a printed circuit board. The memory chips 132 are mounted on the memory board 131 at regular intervals. The module IO ~~bas~~ bus lines 133 are formed on the memory board 131 to be connected to the memory chips 132, respectively. The terminating resistors 134 are formed in the memory chips 132 and connected to ends of the memory bas lines 133, respectively. The stab resistors 135 are formed on the memory board to be connected to other ends of the module IO ~~bas~~ bus lines 133, respectively. The pins 135 are formed at edge on the memory board 131. Each of the stab resistors 135 is also connected to corresponding one of the pins 135.